IN THE CLAIMS

1. (Currently Amended) A memory device including an integrated circuit, the integrated circuit comprising:

~~a data bus;~~

a set of one or more control ports;

a first memory portion comprising a first plurality of storage cells, said first memory portion to be coupled to ~~said~~ a data bus~~, and capable of being cycled once in an amount of time T~~;

a second memory portion comprising a second plurality of storage cells, said second memory portion to be coupled to said data bus~~, and also capable of being cycled once in said amount of time T~~; and

an interface coupled to said set of control ports to receive one or more access requests, said interface to access either said first memory portion or said second memory portion in response to receiving a respective access request and according to portion information in the respective access request, each access request comprising a row command and a column command, said interface ~~capable of receiving~~being configured to receive a complete access request ~~at least one row command and one column command~~ in an amount of time ~~X, where X is~~ less than or equal to ~~T~~a time required to cycle one of the first and second memory portions once.~~;~~

~~wherein said first memory portion may be accessed at any time relative to accessing of said second memory portion, and vice versa.~~

2. (Original) The memory of claim 1, wherein said first and second memory portions are electrically isolated from each other.

3. (Currently Amended) The memory of claim 2, wherein said interface is disposed between said first memory portion and said second memory portion to electrically isolate said first memory portion from said second memory portion~~, and vice versa~~.

4. (Currently Amended) The memory of claim 1, wherein said interface is ~~capable of receiving~~configured to receive concurrently a row command of a first access request to access the first portion and a column command ~~concurrently~~of a second access request to access the second portion.

5. (Original) The memory of claim 1, wherein said interface is capable of receiving a row command and a column command in different halves of a clock cycle.

6. (Original) The memory of claim 1, wherein said memory is a dynamic memory.

7. (Currently Amended) The memory of claim 1, wherein said first memory portion further comprises a first set of sense amplifiers, wherein said second memory portion further comprises a second set of sense amplifiers, and wherein said sets of sense amplifiers are electrically isolated from each other such that noise from activating one set of sense amplifiers does not corrupt data loaded in the other set of sense amplifiers.

8. (Currently Amended) The memory of claim 7, wherein said first and second sets of sense amplifiers are electrically isolated from each other so that activation of said first set of

sense amplifiers ~~may~~ does not corrupt data loaded in ~~be activated at any time relative to activation of~~ said second set of sense amplifiers~~, and vice versa~~.

9. (Currently Amended) The memory of claim 7, wherein said first and second sets of sense amplifiers are electrically isolated from each other so that said first set of sense amplifiers may be activated while said second set of sense amplifiers are loaded with data to be stored in the second memory portion~~there is no required minimum time delay between activating said first set of sense amplifiers and activating said second set of sense amplifiers, and vice versa~~.

10. (Currently Amended) The memory of claim 7, wherein said first and second sets of sense amplifiers are electrically isolated from each other to allow said first and second sets of sense amplifiers ~~may~~ to be activated in consecutive clock cycles.

11. (Currently Amended) The memory of claim 1, wherein said ~~interface receives~~ one or more access requests include a first access request to access said first memory portion[[,]] and a second access request to access said second memory portion, wherein said first access request comprises a first row command[[,]] and said second access request comprises a second row command, and wherein said first and second row commands are received in immediate succession~~said interface is capable of receiving said second row command at any time relative to receiving said first row command~~.

12. (Currently Amended) The memory of claim 1, wherein said ~~interface receives~~one or more access requests include a first access request to access said first memory portion, and a second access request to access said second memory portion, wherein said first access request comprises a first ~~row~~ column command, and said second access request comprises a second ~~row~~ column command, and ~~The memory of claim 11,~~ wherein said first and second column commands are received in immediate succession ~~said interface does not require any minimum time delay between receiving said first row command and receiving said second row command~~.

13. (Currently Amended) The memory of claim 1, wherein ~~said interface receives~~said one or more access requests include a first access request to access said first memory portion, and a second access request to access said second memory portion, wherein said first access request comprises a first row command, and said second access request comprises a second row command, and wherein ~~said interface may receive~~ said first row command and said second row command are received in consecutive clock cycles.

14. (Original) The memory of claim 1, wherein said one or more access requests comprises a read request.

15. (Original) The memory of claim 14, wherein said interface receives and forwards a first access request to said first memory portion, causing said first memory portion to access a first set of data from said first plurality of storage cells, said first set of data having a size no greater than one base granularity, said first memory portion outputting said first set of data onto said data bus, and wherein said interface receives and forwards a second access request to said

second memory portion, causing said second memory portion to access a second set of data from said second plurality of storage cells, said second set of data having a size no greater than one base granularity, said second memory portion outputting said second set of data onto said data bus.

16. (Original) The memory of claim 15, wherein said second set of data follows said first set of data onto said data bus such that there is substantially no idle time on said data bus between said first set of data and said second set of data.

17. (Original) The memory of claim 1, wherein said one or more access requests comprises a write request.

18. (Original) The memory of claim 17, wherein said interface receives and forwards a first access request to said first memory portion, causing said first memory portion to obtain a first set of data from said data bus, said first set of data having a size no greater than one base granularity, said first memory portion storing said first set of data into a subset of said first plurality of storage cells, and wherein said interface receives and forwards a second access request to said second memory portion, causing said second memory portion to obtain a second set of data from said data bus, said second set of data having a size no greater than one base granularity, said second memory portion storing said second set of data into a subset of said second plurality of storage cells.

19. (Original) The memory of claim 18, wherein said second set of data follows said first set of data on said data bus such that there is substantially no idle time on said data bus between said first set of data and said second set of data.

20. (Currently Amended) A memory including an integrated circuit, the integrated circuit comprising:

~~a data bus;~~

a set of one or more control ports;

a first memory portion comprising a first plurality of storage cells, and a first set of sense amplifiers to be coupled ~~to~~ between ~~said~~ a data bus and said first plurality of storage cells, said first memory portion capable of being cycled once in an amount of time T;

a second memory portion comprising a second plurality of storage cells, and a second set of sense amplifiers to be coupled ~~to~~ between said data bus and said second plurality of storage cells, said second memory portion also capable of being cycled once in said amount of time T; and

an interface coupled to said set of control ports to receive one or more access requests, said interface to access either said first memory portion or said second memory portion in response to receiving a respective access request and according to portion information in the respective access request, ~~each access request comprising a row command and a column command,~~ said interface ~~capable of receiving~~being configured to receive at least ~~one~~ a first row command in a first access request and ~~one column~~a second row command in a second access request in an amount of time X, where X is less than or equal to T;

wherein said first row command causes said first set of sense amplifiers ~~may~~ to be activated ~~at any time relative to activation of~~ while said second row command causes said second set of sense amplifiers to be activated~~, and vice versa~~.

21. (Currently Amended) A method for accessing a memory, comprising:

receiving a first access request on a set of one or more control ports, said first access request comprising a first row command;

in response to said first access request, accessing a first set of storage cells in a first portion of said memory;

receiving a second access request on said set of one or more control ports, said second access request comprising a second row command; and

in response to said second access request, accessing a second set of storage cells in a second portion of said memory;

wherein said first row command and second row command are~~may be~~ received within an amount of time not greater than a time required to cycle one of the first and second portions of the memory once~~at any time relative to receiving said first row command~~.

22. (Original) The method of claim 21, wherein said second row command is received immediately after receiving said first row command.

23. (Original) The method of claim 21, wherein said first and second row commands are received in consecutive clock cycles.

24. (Original) The method of claim 21, wherein said first and second portions are electrically isolated from each other.

25. (Currently Amended) The method of claim 21, wherein said first portion comprises a first set of sense amplifiers and said second portion comprises a second set of sense amplifiers, the method further comprising activating~~wherein~~ said first set of sense amplifiers ~~is activated~~ in response to said first access request and activating said second set of sense amplifiers ~~is activated~~ in response to said second access request, ~~and wherein said first set of sense amplifiers may be activated at any time relative to activation of said second set of sense amplifiers, and vice versa~~.

26. (Original) The method of claim 25, wherein said first and second sets of sense amplifiers are electrically isolated from each other such that activation of one set of sense amplifiers does not corrupt data in the other set of sense amplifiers.

27. (Original) The method of claim 25, wherein said second set of sense amplifiers is activated immediately after said first set of sense amplifiers.

28. (Original) The method of claim 25, wherein said first and second sets of sense amplifiers are activated in consecutive clock cycles.

29. (Currently Amended) The method of claim 21, ~~wherein said first portion is capable of being cycled once in an amount of time T, and said second portion is capable of being~~

~~cycled once in said amount of time T,~~ wherein ~~an~~ a respective access request comprises one row command and one column command, and wherein ~~one row command and one column command are~~ a respective access request is received in an amount of time ~~X, where X is~~ less than or equal to ~~T~~the time required to cycle one of the first and second memory portions once.

30. (Currently Amended) The method of claim 29, wherein ~~a~~ the first row command ~~from one~~in the first access request and a column command ~~from another~~in the second access request are received ~~in said amount of time X~~concurrently.

31. (Canceled)

32. (Currently Amended) The method of claim 29, wherein the row and column commands in a respective access request are received in ~~different halves of~~ consecutive clock cycles.

33. (Original) The method of claim 21, wherein said first and second access requests are read requests.

34. (Original) The method of claim 33, wherein accessing said first set of storage cells in said first portion of said memory comprises:

accessing a first set of data from said first set of storage cells, said first set of data having a size no greater than one base granularity; and

outputting said first set of data onto a data bus.

35. (Original) The method of claim 34, wherein accessing said second set of storage cells in said second portion of said memory comprises:

accessing a second set of data from said second set of storage cells, said second set of data having a size no greater than one base granularity; and

outputting said second set of data onto said data bus.

36. (Original) The method of claim 35, wherein said second set of data follows said first set of data onto said data bus such that there is substantially no idle time on said data bus between said first set of data and said second set of data.

37. (Original) The method of claim 21, wherein said first and second access requests are write requests.

38. (Original) The method of claim 37, wherein accessing said first set of storage cells in said first portion of said memory comprises:

obtaining a first set of data from a data bus, said first set of data having a size no greater than one base granularity; and

storing said first set of data into said first set of storage cells.

39. (Original) The method of claim 37, wherein accessing said second set of storage cells in said second portion of said memory comprises:

obtaining a second set of data from said data bus, said second set of data having a size no greater than one base granularity; and

storing said second set of data into said second set of storage cells.

40. (Original) The method of claim 39, wherein said second set of data follows said first set of data on said data bus such that there is substantially no idle time on said data bus between said first set of data and said second set of data.

41-42. (Canceled)

43. (Currently Amended) In a memory system wherein a memory comprises a first portion and a second portion, a method for controlling access to said memory, comprising:

deriving a first access request to access said first portion of said memory, said first access request comprising a first row command;

deriving a second access request to access said second portion of said memory, said second access request comprising a second row command;

sending said first row command to said memory; and

sending said second row command to said memory;

wherein said first row command and said second row command ~~may be~~are sent within a time not greater than a time T required to cycle one of the first and second portions of the memory once~~at any time relative to sending said first row command such that no relative timing constraints are imposed between sending said first row command and sending said second row command~~.

44. (Original) The method of claim 43, wherein said second row command is sent immediately after said first row command.

45. (Original) The method of claim 43, wherein said first and second row commands are sent in consecutive clock cycles.

46. (Original) The method of claim 43, wherein each access request comprises one row command and one column command.

47. (Currently Amended) The method of claim 46, ~~wherein each of said first and second portions of said memory is capable of being cycled once in an amount of time T, and~~ wherein ~~said second~~the row command and ~~a~~ the column command of a respective access request are sent to said memory in an amount of time ~~X, where X is~~ less than or equal to T.

48. (Currently Amended) The method of claim 47, wherein said second row command and ~~said~~ a column command of the first access request are sent concurrently.

49. (Currently Amended) The method of claim 47, wherein said second row command and ~~said~~ a column command of the first access request are sent in different halves of a clock cycle.

50. (Original) The method of claim 47, wherein said column command is a first column command associated with said first access request.

51. (Currently Amended) In a memory system wherein a memory ~~comprises a plurality of memory portions~~device in an integrated circuit is accessible through a memory bus, a method for controlling access to said memory, comprising:

deriving a first access request, said first access request being directed to a first memory portion of said memory device;

sending said first access request to said memory device for processing, said first access request causing first data to be read out of or written into said first memory portion, said first data being of one base granularity in size;

deriving a second access request;

determining whether said second access request is directed to said first memory portion; and

in response to a determination that said second access request is not directed to said first memory portion, sending said second access request to said memory device, said second access request causing second data to be read out of or written into a second memory portion, said second data being of one base granularity in size, wherein said sending of said second access request is timed such that said second data follows said first data on said memory bus with substantially no idle time in between ~~need not be constrained by when said first access request was sent~~.

52. (Currently Amended) The method of claim 51, wherein said first access request comprises a first row command and said second access request comprises a second row command, and wherein ~~there is no required minimum time delay between sending~~ said first row command and said second row command are sent within a time not greater than a time required to cycle one of said first and second memory portions once.

53. (Original) The method of claim 52, wherein said second row command is sent immediately after said first row command.

54. (Original) The method of claim 52, wherein said first and second row commands are sent in consecutive clock cycles.

55. (Currently Amended) The method of claim 51, further comprising:

in response to a determination that said second access request is directed to said first memory portion, ~~ensuring that a minimum amount of time has passed since said first access request was sent; and~~

sending said second access request to said memory after ~~said~~ a minimum amount of time has passed, said minimum amount of time being at least the time required to cycle one memory portion once.

56 - 61. (Canceled)

62. (Currently Amended) A memory system, comprising:

a data bus,

a memory device in an integrated circuit, comprising:

~~a data bus;~~

a set of one or more control ports;

a first memory portion comprising a first plurality of storage cells, said first memory portion coupled to said data bus, and capable of being cycled once in an amount of time T;

a second memory portion comprising a second plurality of storage cells, said second memory portion coupled to said data bus, and also capable of being cycled once in said amount of time T; and

an interface coupled to said set of control ports to receive one or more access requests to access either said first memory portion or said second memory portion, each access request comprising a row command and a column command, said interface ~~capable of receiving at least one row command and one column command~~is configured to receive a complete access request in an amount of time X, where X is less than or equal to T;

~~wherein said first memory portion may be accessed at any time relative to accessing of said second memory portion, and vice versa;~~ and

a controller coupled to said data bus and said set of one or more control ports to control operation of said memory device, said controller ~~capable of sending~~configured to send a complete access request ~~at least one row command and one column command to said memory~~ in an amount of time that is substantially the same as said amount of time X~~, and capable of sending a first row command to access said~~

~~first memory portion and a second row command to access said second memory portion at any time relative to each other such that no relative timing constraints are imposed between sending said first row command and sending said second row command~~.

63. (Original) The memory system of claim 62, wherein said first and second memory portions are electrically isolated from each other.

64. (Original) The memory system of claim 63, wherein said interface is disposed between said first memory portion and said second memory portion to electrically isolate said first memory portion from said second memory portion, and vice versa.

65. (Currently Amended) The memory system of claim 62, wherein said controller ~~sends said second row command immediately after sending said first row command.~~ is further configured to:

derive a first access request, said first access request being directed to said first memory portion;

send said first access request to said memory device for processing, said first access request causing first data to be read out of or written into said first memory portion, said first data being of one base granularity in size;

derive a second access request;

determine which memory portion said second access request is directed to; and

send said second access request to said memory in response to a determination that said second access request is directed to said second memory portion, said second access request causing second data to be read out of or written into said second memory portion, said second data being of one base granularity in size, wherein said second access request is sent within such a time after sending said first access request that said second data follows said first data on the memory bus with substantially no idle time in between.

66. (Currently Amended) The memory system of claim 62, wherein said first access request includes a first row command and said second access request includes a second row command, and wherein said controller sends said first and second row commands ~~in consecutive clock cycles~~within an amount of time that is substantially the same as said amount of time X.

67. (Currently Amended) The memory system of claim 66, wherein said memory is configured to allow said first and second memory portions ~~may~~ to be accessed in consecutive clock cycles.

68. (Currently Amended) The memory system of claim 62, wherein said first memory portion further comprises a first set of sense amplifiers, and said second memory portion further comprises a second set of sense amplifiers, and wherein said memory device is configured to allow said first set of sense amplifiers ~~may~~ to be activated ~~at any time relative to activation of~~ within the time X after said second set of sense amplifiers are activated~~, and vice versa~~.

69. (Original) The memory system of claim 68, wherein said first and second sets of sense amplifiers are electrically isolated from each other.

70. (Currently Amended) The memory system of claim 68, wherein said memory is configured to require~~there is~~ no ~~required~~ minimum time delay between activating said first set of sense amplifiers and activating said second set of sense amplifiers~~, and vice versa~~.

71. (Currently Amended) The memory system of claim ~~68~~66, wherein said controller sends said first and second row commands in consecutive clock cycles.

72. (Currently Amended) The memory system of claim 71, wherein said memory is configured to allow said first set of sense amplifiers and said second set of sense amplifiers ~~may~~ to be activated in consecutive clock cycles.

73. (New) A memory device in an integrated circuit to be coupled to a data bus, comprising:

a first memory portion comprising a first plurality of storage cells;

a second memory portion comprising a second plurality of storage cells; and

an interface to receive a plurality of access requests, each access request for accessing one of said first and second memory portions and including a column command, said plurality of access requests being timed such that a first column command for accessing said first memory portion and a second column command for accessing said second memory portion are

both received by said interface in a time period not longer than an amount of time required to cycle one of the first and second memory portion once.

74. (New) The memory device of claim 73 wherein said amount of time required to cycle one of the first and second memory portions once is substantially equal to an amount of time needed to read one base granularity of data out of said one of the first and second memory portions.

75. (New) The memory device of claim 73 wherein said first and second column command are from first and second read requests and cause first data of one base granularity in size from said first memory portion and second data of one base granularity in size from said second memory portion to be placed on said data bus, said second data follows said first data with substantially no idle time in between.

76. (New) The memory device of claim 73 wherein said first and second column commands are from first and second write requests and cause first data of one base granularity in size from said data bus and second data of one base granularity in size from said data bus to be placed in respective ones of said first and second memory portions, said second data follows said first data on said data bus with substantially no idle time in between.

77. (New) The memory device of claim 73 wherein the first and second column commands are received in consecutive clock cycles.

78. (New) A memory device in an integrated circuit to be coupled to a data bus, comprising:

a first memory portion;

a second memory portion;

an interface to receive access requests and to forward respective access requests to respective ones of said first and second memory portions, said access requests including a first access request causing first data to be read out of or written into said first memory portion and a second access request causing second data to be read out of or written into said second memory portion, said first data being of one base granularity in size, said second data being of one base granularity in size and following said first data on said memory bus with substantially no idle time in between.

79. (New) The memory device of claim 78 wherein said first access request includes a first column command and said second access request includes a second column command, and wherein said interface is configured to receive both said first and second column commands within a time period not longer than an amount of time required to cycle one of said first and second memory portions once.

80. (New) The memory device of claim 79 wherein said amount of time required to cycle one of the first and second memory portions once is substantially equal to an amount of time needed to read one base granularity of data out of said one of the first and second memory portions.

81. (New) The memory device of claim 79 wherein said first and second column commands are received in consecutive clock cycles.

82. (New) A method performed by a memory device in an integrated circuit coupled to a data bus, comprising:

receiving a first access request at said memory device, said first access request for accessing a first memory portion of said memory device and including a column command;

in response to said first access request, writing first data from said data bus into said first portion of said memory, said first data being of one base granularity in size;

receiving a second access request at said memory device, said second access request for accessing a second memory portion of said memory device and including a second column command; and

in response to said second access request, writing second data from said data bus into said second portion of said memory, said second data being of one base granularity in size;

wherein said first and second column commands are received within such a time period that said second data follows said first data on said data bus with substantially no idle time in between.

83. (New) The method of claim 82, wherein said time period is not longer than an amount of time required to cycle one of the first and second portions of the memory device once.

84. (New) The memory device of claim 83 wherein said amount of time required to cycle one of said first and second memory portions once is substantially equal to an amount of

time needed to write one base granularity of data into one of said first and second memory portions.

85. (New) A method performed by a memory device in an integrated circuit coupled to a data bus, comprising:

receiving a first access request;

in response to said first access request, placing first data from a first memory portion of said memory device on said data bus, said first data being of one base granularity in size;

receiving a second access request; and

in response to said second access request, placing second data from a second memory portion of said memory device on said data bus, said second data being of one base granularity in size;

wherein said second data follow said first data on said data bus with substantially no idle time in between.

86. (New) The method of claim 85 wherein said first access request includes a first column command and said second access request includes a second column command, and wherein said first and second column commands are both received by said memory device within a time period not longer than an amount of time required to cycle one of said first and second memory portions once.

87. (New) The method of claim 86 wherein said amount of time required to cycle one of the first and second memory portions once is substantially equal to an amount of time needed to read one base granularity of data out of said one of the first and second memory portions.

88. (New) The method of claim 87 wherein said first and second column commands are received in consecutive clock cycles.

89. (New) A method for accessing an integrated circuit memory device, comprising:

deriving a first access request to access a first memory portion of said memory device, said first access request including a first column command;

deriving a second access request to access a second memory portion of said memory device, said second access request comprising a second column command;

sending said first column command to said memory device; and

sending said second column command to said memory device within such a time after sending said first column command that said first and second column commands are both received by said memory device within a period of time not longer than a time required to cycle one of said first and second memory portions once.

90. (New) The method of claim 89 wherein said memory is coupled to a data bus and wherein said amount of time required to cycle one of the first and second memory portions once is substantially equal to an amount of time needed to place one base granularity of data out of said one of the first and second memory portions onto said data bus.

91. (New) The method of claim 43, wherein said first and second row commands are sent in consecutive clock cycles.